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09/866,800	05/30/2001	Kazuhiko Okawa	109657	5674

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/866,800	Applicant(s) OKAWA ET AL.	
	Examiner Johannes P Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8, 17* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statem nt

The examiner has considered the items listed in the Information Disclosure Statement of Paper No.17. Also enclosed is a signed copy of the Information Disclosure Statement of May 2001, Paper No. 8, as requested by Applicant.

Response to Amendment

Amendment C filed 03/07/03 and entered as Paper No. 18 forms the basis of this office action. In said Amendment C Applicant substantially amended the claim language of all independent claims (1 and 20). On the basis thereof new art rejections are herewith submitted. As a courtesy to Applicant a translation by the USPTO translators of Natori (JP406204475A) will be faxed to Applicant's representative as soon as it will become available.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1-4 and 25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Natori (JP406204475A) in view of S. Wolf et al (ISBN 0-961672-3-7) and S. Wolf (ISBN 0-961672-5-3). Natori teaches a semiconductor device comprising: a

semiconductor substrate 8 (cf. section [0027]); a MOS transistor (cf. sections [0002] – [0004]), MOSFET 10, formed on the semiconductor substrate (cf. English abstract, Constitution, first sentence) and includes a first diffusion region 9 (English abstract, "Constitution", first sentence); a first isolation region (region most to the left on Figure 2c) which isolates the MOS transistor from other MOS transistors such as disclosed MOS transistor 20 (cf. section [0024]) on the semiconductor substrate; a second isolation region formed between the MOS transistor and the first isolation region (second isolation region is isolation region 4 centrally positioned in Figure 2c); a second diffusion region 9 (abutting the said second isolation region) which is formed in a region isolated by the second isolation region from the said MOS transistor 10 and which, by virtue of its N type conductivity (cf. first sentence of English abstract, "Constitution" and section [0024], first sentence) makes up a lateral bipolar transistor in the semiconductor substrate (because said substrate is of P-type conductivity, see section [0017]) and the first diffusion region of the MOS transistor (i.e., a lateral NPN bipolar transistor); and a third diffusion region 11 (cf. first sentence of "Constitution", English abstract) formed at a deeper position of the first diffusion region near the second isolation region (cf. Figure 2c) and (because of its P-conductivity type) makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

Natori does not necessarily teach the further limitations that

(a) a silicide layer should be formed on a surface of the semiconductor substrate excluding the first and second isolation region, and

(b) the role of the substrate be substituted for that of a well.

However, it would have been obvious to include the teaching ad (a) in view of Wolf et al, who teach the application of silicide on top of the source/drain regions for the specific purpose to reduce the sheet resistance (see pages 397-399), which constitutes a general advantage for higher operational speed and decreased ohmic loss and heat production. Furthermore, it would have been obvious to include the teaching ad (b) in view of Wolf who teaches formation of wells for each of the MOSFETs in a CMOS application of MOSFET technology (cf. pages 523-527).

Motivation to include this teaching by Wolf et al on applying the silicide in the invention by Natori stems from this general advantage of higher speed and reduced ohmic loss and heat. *Combination* of said teaching with said invention is straightforward through the standard process of salicide formation (self-aligned silicide formation process) (see Wolf et al, pages 397-399). *Success* in implementing said combination can therefore be reasonably expected.

Motivation to include the teaching by Wolf on the formation of a well in the invention by Natori is the application of the additionally protected device as taught by Natori to the MOSFETs that form CMOSFET devices, which is a standard application of MOSFETs. *Combination* of said teaching with said invention is straightforward because well technology is well established. *Success* of the implementation of the combination can therefore be reasonably expected.

With regard to claim 2: the breakdown strength of the Zener diode as taught by Natori is designed to be reduced to, or lower than, the insulation breakdown strength of the gate insulation film (cf. Abstract, "Constitution", lines 5-9), i.e., the breakdown start

voltage of the MOS transistor. The inequality between the breakdown strengths of claim 2 is a necessary requirement for the device specification of Natori to exert any protective function. The further limitation as defined by claim 2 thus does not distinguish over the primary reference.

With regard to claim 3: in the device essentially taught by Natori in view of Wolf et al, an NPN lateral bipolar transistor is formed by the first and second diffusion regions which are N-type diffusion regions (see above under claim 1; see also Natori, section [0017]) and a P-type well (as taught by Wolf et al to substitute for the P-type substrate in Natori) (cf. section [0017]); the MOS transistor having the first diffusion region is an N-type MOS transistor (see section [0017] which sets a potential of a pad to a low potential; and the third diffusion region which makes up the Zener diode by the junction with the first diffusion region is a P-type diffusion region (see section [0017]). Therefore, the further limitations defined by claim 3 do not distinguish over the prior art cited for the claim on which it depends (claim 1).

With regard to claim 4: it is understood in the art of semiconductor device technology that an overall interchange of all conductivity types in a semiconductor device is a matter of design choice, unless Applicant shows in the disclosure that said reversal is critical to the invention. Applicant has not done that. In the underlying case, the device of claim 4 is obtained from the device of claim 3 by full and systematic interchange of all conductivity types.

With regard to claim 25: the first diffusion region in the device by Natori forms the drain of the MOS transistor 10 (cf. section [0017]). Therefore, the further limitation of claim 25 does not distinguish over the prior art as offered by the primary reference.

3. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Natori and Wolf et al as applied to claim 1 above, and further in view of Uchizumi et al (JP406224376A). Neither Natori nor Wolf et al teach the further limitation of claim 5. However, the incorporation of an additional impurity diffusion region adjacent a source or drain diffusion region and of opposite conductivity type as that of said source or drain region in a MOSFET device, such that said additional impurity diffusion region is in contact with a silicide layer has long been recognized in the art of protection devices for MOSFET's, as evidenced by Uchizumi et al, who teach an N-type conductivity diffusion region 14 in close proximity with a source region of an NMOS device by ion implantation (cf. "Constitution", lines 2-4), for the *specific purpose* of preventing latch-up protection (cf. "Purpose", lines 1-2). Said purpose is relevant to any CMOS semiconductor device and thus provides *motivation* to include the teaching by Uchizumi et al in the invention as essentially taught by Natori and Wolf et al, while combinability of said teaching with said invention is straightforward and can be directly implemented in the device by Natori et al through (e.g., phosphorus) ion implantation. *Success* in implementation the teaching by Uchizumi et al in this regard can therefore be reasonably expected.

4. ***Claims 6-7*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Natori, Wolf et al, and Wolf as applied to claim 3 above, and further in view of Amerasekera (5,949,094). As detailed above, claim 3 is unpatentable over Natori in view of Wolf et al and Wolf. None of the latter necessarily teach the further limitation of claim 6.

However, the implementation of bipolar transistors for the *specific purpose* of protection against electrostatic discharge (ESD) has long been patented, as evidenced by Amerasekera et al, who teach a NPN bipolar transistor (N.B.: interchange of N and P regions is standardly recognized in the art as having no patentable weight) (cf. title and abstract) through N regions 18 and 20 adjacent to each other, P region 14 underneath them, and N region 106 underneath 14. The invention taught by Amerasekera pertains to an ESD protection device including the NPN bipolar transistor component, or in the alternative PNP transistor component, irregardless of the nature of the semiconductor device that is to be protected, but would readily apply to the case of a MOS transistor.

Therefore, the *motivation* for the formation of fourth and fifth diffusion regions formed between the silicide layer and the third diffusion region so that said third, fourth, and fifth diffusion regions make up a PNP bipolar transistor would have been an obvious additional precaution against ESD for anyone with ordinary skills in the art of semiconductor ESD protection devices. The teaching in this regard by Amerasekera can be combined with the invention as essentially taught by Natori and Wolf by straightforward application of the same tools for creating diffusion regions in Natori in the first place, namely implantation. Therefore, it would have been obvious to one of

ordinary skills in the art to modify the invention as defined by either claim 3 or claim 4 at the time said invention was made so as to include the further limitations defined by claims 6 and 7, respectively.

5. ***Claim 20-23 and 26*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Natori (JP406204475A) in view of S. Wolf et al (ISBN 0-961672-3-7) and Wolf (ISBN 0-961672-5-3). Natori teaches a semiconductor device comprising:

a semiconductor substrate 8 (cf. section [0027]);

a MOS transistor (cf. sections [0002] – [0004]), MOSFET 10, formed on the semiconductor substrate (cf. English abstract, Constitution, first sentence) and includes a first diffusion region 9 (English abstract, "Constitution", first sentence);

a first isolation region (region most to the left on Figure 2c) which isolates the MOS transistor from other MOS transistors such as disclosed MOS transistor 20 (cf. section [0024]) on the semiconductor substrate;

a second isolation region formed between the MOS transistor and the first isolation region (second isolation region is isolation region 4 centrally positioned in Figure 2c);

a second diffusion region 9 (abutting the said second isolation region) which is formed in a region isolated by the second isolation region from the said MOS transistor 10 and which, by virtue of its N type conductivity (cf. first sentence of English abstract, "Constitution" and section [0024], first sentence) makes up a lateral bipolar transistor in the semiconductor substrate (because said substrate is of P-type conductivity, see

section [0017]) and the first diffusion region of the MOS transistor (i.e., a lateral NPN bipolar transistor);

a third diffusion region 11 (cf. first sentence of "Constitution", English abstract) formed between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and makes up a Zener diode by the PN junction together with the first diffusion region (cf. Figure 2c) and (because of its P-conductivity type) makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

Natori does not necessarily teach the further limitations that

(a) a silicide layer should be formed on a surface of the semiconductor substrate including the first and second isolation region and a region connecting the first and third diffusion regions, and

(b) the role of the substrate be substituted for that of a well.

However, it would have been obvious to include the teaching ad (a) in view of Wolf et al, who teach the application of silicide on top of all source/drain regions for the specific purpose to reduce the sheet resistance (see pages 397-399), which constitutes a general advantage for higher operational speed and decreased ohmic loss and heat production. Please note that consistent application of the teaching by Wolf to cover all source/drain regions (cf. Figure 13-c and discussion on page 398 in the final paragraph) implies that in Natori a region will be covered that includes the isolation regions, although this does not mean the isolation regions themselves are covered with silicide (nor is this disclosed in the application by Applicant). Furthermore, it would have been

obvious to include the teaching ad (b) in view of Wolf et al who teach formation of wells for each of the MOSFETs in a CMOS application of MOSFET technology (cf. pages 816-818).

Motivation to include this teaching under ad (a) by Wolf et al in the invention by Natori stems from this general advantage of higher speed and reduced ohmic loss and heat. *Combination* of said teaching with said invention is straightforward through the standard process of salicide formation (self-aligned silicide formation process) (see Wolf et al, page 834). *Success* in implementing said combination can therefore be reasonably expected.

Motivation to include the teaching by Wolf on the formation of a well (ad (b)) in the invention by Natori is the application of the additionally protected device as taught by Natori to the MOSFETs that form CMOSFET devices, which is a standard application of MOSFETs. *Combination* of said teaching with said invention is straightforward because well technology is well established. *Success* of the implementation of the combination can therefore be reasonably expected.

With regard to claim 21: the breakdown strength of the Zener diode as taught by Natori is designed to be reduced to, or lower than, the insulation breakdown strength of the gate insulation film (cf. Abstract, "Constitution", lines 5-9), i.e., the breakdown start voltage of the MOS transistor. The inequality between the breakdown strengths of claim 2 is a necessary requirement for the device specification of Natori to exert any protective function. The further limitation as defined by claim 2 thus does not distinguish over the primary reference.

With regard to claim 22: in the device essentially taught by Natori in view of Wolf et al, an NPN lateral bipolar transistor is formed by the first and second diffusion regions which are N-type diffusion regions (see above under claim 21; see also Natori, section [0017]) and a P-type well (as taught by Wolf et al to substitute for the P-type substrate in Natori) (cf. section [0017]); the MOS transistor having the first diffusion region is an N-type MOS transistor (see section [0017] which sets a potential of a pad to a low potential; and the third diffusion region which makes up the Zener diode by the junction with the first diffusion region is a P-type diffusion region (see section [0017]). Therefore, the further limitations defined by claim 22 do not distinguish over the prior art cited for the claim on which it depends (claim 21).

With regard to claim 23: it is understood in the art of semiconductor device technology that an overall interchange of all conductivity types in a semiconductor device is a matter of design choice, unless Applicant shows in the disclosure that said reversal is critical to the invention. Applicant has not done that. In the underlying case,

the device of claim 23 is obtained from the device of claim 22 by full and systematic interchange of all conductivity types.

With regard to claim 26: the first diffusion region in the device by Natori forms the drain of the MOS transistor 10 (cf. section [0017]). Therefore, the further limitation of claim 25 does not distinguish over the prior art as offered by the primary reference.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gilbert et al (5,920,774); Wu (5,920,774).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
May 15, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800